REMARKS/ARGUMENTS

Claims 1-2, 4-6, 8-11, 13-19, 21-23 and 25-26 are pending in this application. Claims 3, 7, 12, 20 and 24 have been canceled without prejudice. Claims 1, 15-16, 18, 21-23 and 25 have been currently amended. Claims 1 and 15 are independent claims. Support for the amendment may be found throughout the specification and drawings.

Claim Rejections – 35 USC § 103(a)

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige et al. ("Nagashige", U.S. Patent Number 5,313,588), Wilson et al. ("Wilson", U.S. Patent Number 6,738,821) and Blumenau ("Blumenau", U.S. Patent Number 6,263,445). Claims 2-3 and 5-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson and Blumenau in view of Richardson ("Richardson", U.S. Patent Number 6,205,506). Claims 4 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Richardson and further in view of Su et al. ("Su", U.S. Patent Number 6,047,339). Claims 9 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson and Blumenau in view of Morris et al. ("Morris", U.S. Patent Number 6,434,650). Claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Morris in view of Daniel et al. ("Daniel", U.S. Patent Number 5,726,985). Claims 12-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Morris in view of Su. Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Su. Claims 16-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Su in view of Richardson. Claims 20-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Su in view of Kang ("Kang", U.S. Patent Number 6,052,133). Claims 25-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagashige, Wilson, Blumenau, Su and Kang in view of Daniel. Applicant respectfully traverses these rejections.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references

themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (emphasis added) (MPEP § 2143). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. (emphasis added) *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicant herein respectfully submits that independent Claims 1 and 15 were not taught, disclosed, or suggested by any reference cited by the Patent Office (i.e., Nagashige, Wilson, Su, Morris, Daniel, Blumenau and Kang) or any combination of these references.

Moreover, Applicant cannot agree with the Patent Office's assertion that Su "teaches a plurality of memory banks, which are equivalent to the bus operation information structures, that each includes a status flag that can be used to indicate ownership of the corresponding bank (See Column 4 Lines 30-32, Column 5 Lines 38-39, and Column 5 Lines 52-54); the writer controller, which is equivalent to the processor, setting the status flag to a value of 'start', which is equivalent to setting the owner field to the sequencer, upon writing data to the memory bank, which is equivalent to forming a bus operation information structure (See Column Lines 33-34)" (Office Action dated 11/15/2004, page 16, lines 2-9; also see page 19, bottom 6 lines to page 20, top 4 lines).

As indicated in Column 3, Lines 37-39 of Su, "a single FIFO memory device 31 is partitioned into N distinct memory regions ("banks") 32-1, 32-2, . . . 32-N by a controller 35" (emphasis added). In other words, Su's memory banks are actually "memory spaces" in Claims 1 and 15 and *cannot* be "bus operation information structures" in Claims 1 and 15.

Furthermore, as indicated in Column 3, Lines 63-64 of Su, "[a] write controller 42 manages the flow of data into the banks 32-1, 32-2, ... 32-N" (emphasis added). In other words, Su's writer controller manages the flow of data into the memory banks (i.e., "memory spaces" in Claims 1 and 15) and thus *cannot* form a bus operation information structure which includes a command, data and an owner field indicating whether the processor or the sequencer has control over the bus operation

information structure. Therefore, Su's writer controller *cannot* be the "processor" in Claims 1 and 15.

Applicant herein respectfully reminds the Patent Office that Su's status flags *cannot* be analogized to "owner fields" in Claims 1 and 15 since an "owner field" is included in a bus operation information structure according to Claims 1 and 15. In comparison, as indicated in Column 4, Lines 7-13, "[e]ach bank 32-1, 32-2, . . . 32-N has at least two associated status flags: a "done" flag 34-1, 34-2, . . . 34-N that indicates to the write controller 42 that the corresponding bank 32-1, 32-2, . . . 32-N is empty and can accept data from a writing device; and a "start" flag 36-1, 36-2, . . . 36-N that indicates to the read controller 44 that the corresponding bank is full and therefore can provide data to a reading device" (emphasis added). In other words, Su's status flags are *associated* with each memory bank (i.e., memory space in Claims 1 and 15). Nowhere in Su is it disclosed, taught or suggested that Su's status flags are included in a bus operation information structure.

At least based on the foregoing described reasons, the rejection of Claims 1 and 15 should be withdrawn, and Claims 1 and 15 should be allowed.

Claims 2, 4-6, 8-11 and 13-14 depend from Claim 1 and are therefore allowable due to their dependence. Claims 16-19, 21-23 and 25-26 depend from Claim 15 and are therefore allowable due to their dependence.
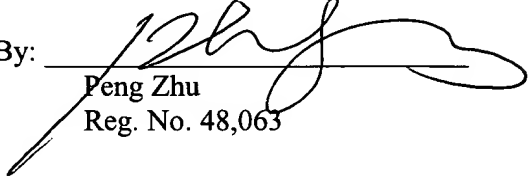
CONCLUSION

In light of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in the case.

Respectfully submitted on behalf of

LSI Logic Corporation,

Dated: December 16, 2004

By: _____

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